Review Vol. 16, No. 4 / 1 Apr 2026 / Optical Materials Express 793

Optical Materials EXPRESS

Fast-track process development: using semiconductor platforms to accelerate semiconductor progress [Invited]

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Abstract: Semiconductor innovation is increasingly constrained by the complexity, cost, and time involved in developing and optimizing advanced manufacturing processes. Traditional R&D approaches anchored in sequential experimentation and tool-specific workflows create critical bottlenecks that impede progress across the full spectrum of semiconductor technologies, including deposition, patterning, etching, doping, and integration. In this perspective, we present a new paradigm: leveraging semiconductor platforms themselves as engines for accelerating their own advancement. We introduce the **EMPOWEr** framework—**E**xpedited **M**anufacturing **P**rocess **O**ptimization through **W**afer-scale **E**xpe**r**imentation—which reimagines semiconductor wafers not as passive substrates, but as programmable experimental platforms enabling massively parallel process exploration. By embedding controlled process variability and integrated characterization directly into wafer-scale infrastructure, EMPOWEr addresses long-standing bottlenecks in process optimization, expands the materials and methods accessible to backend integration, and opens new pathways toward agile, scalable, and sustainable semiconductor innovation. This perspective outlines how EMPOWEr can transform semiconductor R&D into a self-reinforcing, high-throughput ecosystem, accelerating both the pace and scope of next-generation microfabrication.

1. Introduction

The relentless advancement of semiconductor technology hinges critically on rapid development and refinement of manufacturing processes. As device architectures evolve toward increasingly complex and heterogeneous systems encompassing logic, memory, photonics, and sensing functionalities, process development has emerged as a fundamental bottleneck constraining the innovation pipeline. New materials must simultaneously satisfy stringent performance criteria while maintaining compatibility with existing integration flows, thermal budgets, and foundry specifications. Concurrently, optimization of deposition, patterning, etching, doping, and annealing processes requires navigation of vast, multidimensional parameter spaces characterized by intricate interdependencies. Traditional sequential approaches to process iteration impose substantial demands on time, labor, and tool resources, particularly when conducted at full-wafer scales, creating inefficiencies that compound across the development cycle.

For instance, developing a thin-film deposition process for a novel material system typically requires systematic exploration of dozens of interdependent variables, including gas composition, pressure, substrate temperature, power levels, and temporal sequences. Each process condition must be validated through film growth and subsequently characterized using techniques such

#581635 https://doi.org/10.1364/OME.581635
Journal © 2026 Received 21 Oct 2025; revised 6 Feb 2026; accepted 6 Feb 2026; published 3 Mar 2026

as X-ray diffraction, ellipsometry, or electron microscopy. Even with modest parameter sets, this workflow can consume hundreds of wafers and hundreds of tool-hours, underscoring the substantial investment required for each integration effort. Industry analyses indicate that the complete development cycle for a new deposition material—from initial pathfinding and concept validation through device integration and manufacturing ramp-up—spans one to four and a half years, with one to three years typically required to achieve initial process integration alone [1]. This protracted timeline reflects the cumulative burden of iterative experimentation across each development phase, creating fundamental inefficiencies that limit the pace of semiconductor innovation.

Combinatorial experimentation has emerged as a promising approach to circumvent these bottlenecks. However, traditional combinatorial materials science has predominantly focused on compositional screening, employing co-deposition or spatial gradients to identify optimal multi-component systems [2]. By contrast, extending combinatorial strategies to encompass processing variables has remained comparatively underdeveloped. Notable demonstrations include using substrate temperature gradients to screen film deposition or annealing parameters [3–8], spatially varied ion implantation to synthesize nanostructures [9,10], and staged plasma exposure for etching optimization [11]. Yet these approaches rely on bulky, externally controlled instrumentation such as custom masks, scanned laser systems, or reconfigured plasma sources, which impose significant limitations on flexibility, scalability, and foundry compatibility.

On another front, recent developments in autonomous or self-driving laboratories have demonstrated promising advances in accelerating thin-film process development through closed-loop experimentation, *in situ* diagnostics, and machine learning-guided optimization [12–14]. However, these platforms typically require customized deposition tools, bespoke robotic infrastructure, or substantial retrofitting of existing systems, resulting in high cost and limited compatibility with standard semiconductor manufacturing environments. Moreover, despite their automation, most self-driving labs remain constrained by inherently serial experimental workflows, where process conditions are varied one sample at a time. As a result, throughput remains relatively low, and the cumulative time and resource burden associated with exploring high-dimensional process spaces remains significant.

Beyond the time and resource demands of process optimization, new material integration into semiconductor manufacturing faces formidable compatibility challenges. Even when a material exhibits compelling electronic, optical, or structural properties, its practical adoption is often hindered by constraints imposed by existing process flows—most notably, the backend thermal budget. In advanced complementary metal–oxide–semiconductor (CMOS) fabrication, backend-of-the-line (BEOL) integration imposes limits on thermal exposure to prevent degradation of interconnects and previously fabricated device layers. The allowable BEOL thermal budget typically ranges from ~350 to 450 °C, depending on the Cu/low-k stack design and associated reliability requirements. However, many emerging material systems such as ferroelectrics, magnetic oxides, and two-dimensional (2D) semiconductors require high-temperature growth or post-deposition annealing to realize their target properties. This mismatch can disqualify otherwise promising materials from practical deployment. Moreover, integration constraints extend beyond thermal limits to include plasma compatibility, contamination control, mechanical stress management, and conformality over complex topographies. These issues necessitate extensive process adaptation and often bespoke tool modifications, further impeding development timelines and reducing cross-platform compatibility prospects.

We introduce **EMPOWEr** (**E**xpedited **M**anufacturing **P**rocess **O**ptimization through **W**afer-scale **E**xpe**r**imentation) as a paradigm to address both the complexity of process development and the barriers to material integration in semiconductor manufacturing. EMPOWEr leverages the precision and scalability of semiconductor microsystems technology to transform wafers from passive substrates into active, programmable testbeds. By embedding spatially addressable microstructures capable of locally modulating process conditions directly onto standard wafers, EMPOWEr enables massively parallel and spatially localized experimentation within foundry-compatible infrastructure. Prior demonstrations using microfabricated resistive heaters ("microhotplates") for combinatorial control of film growth temperatures represent early realizations of this concept [15–19]. The local processing capability is particularly critical for BEOL integration, as it allows high-temperature or otherwise incompatible steps to be confined to micrometer-scale regions, without violating global process constraints. Crucially, EMPOWEr enables developers to evaluate new materials and processes in a form factor and operational context that are inherently compatible with existing toolsets and workflows. In doing so, it not only accelerates the optimization of complex process spaces but also opens a practical pathway for integrating previously inaccessible materials into advanced semiconductor platforms. In the following section, we detail the architectural and operational principles of this platform and outline how it enables a self-reinforcing, high-throughput ecosystem for semiconductor innovation.

2. Platform for parallel and localized process exploration

The EMPOWEr framework is instantiated through the On-Wafer Lab (OWL), a wafer-scale experimental platform built on standard semiconductor foundry infrastructure. Unlike many emerging self-driving lab architectures that rely on highly customized and expensive instrumentation, OWL leverages lithographically defined microsystems that can be readily integrated with existing CMOS process flows and toolsets. This approach avoids the need for custom-built equipment or extensive retrofitting, offering a cost-effective and scalable solution for high-throughput experimentation. OWL transforms the wafer into a high-density array of programmable experimental units, each capable of locally modulating process parameters such as temperature, substrate bias, plasma excitation, or optical input. These independently addressable micro-environments enable simultaneous, spatially resolved exploration of large process parameter spaces on a single wafer. Following processing, material responses across the array can be characterized using high-throughput, spatially resolved techniques, converting a single wafer run into a rich combinatorial dataset. This architecture compresses weeks of serial experimentation and hundreds of wafer runs into one integrated workflow, substantially accelerating process optimization while remaining fully compatible with existing semiconductor manufacturing infrastructure.

The OWL platform is inherently versatile and broadly applicable across a wide range of semiconductor processes. Figure 1 depicts an embodiment of OWL applied to thin film deposition. Its modular, programmable architecture supports integration with diverse processing modalities, including various physical vapor deposition (PVD) and chemical vapor deposition (CVD) techniques. Beyond *in situ* parameter control during deposition, OWL enables localized post-deposition treatments such as thermal annealing, plasma exposure, and electric or magnetic field activation, facilitating process steps critical to phase transformation, stress engineering, crystallinity control, and interface tuning. The same infrastructure can be extended to plasma etching applications, where spatially resolved biasing, plasma or surface conditioning may enable combinatorial pattern transfer studies. Furthermore, OWL can be coupled with characterization techniques such as electron microscopy or scanning spectroscopy to perform high-throughput, *in situ* imaging or mapping of material transformations. In essence, OWL provides a universal, wafer-scale platform for accelerating development and integration of process technologies spanning the full semiconductor fabrication stack.

The OWL platform is designed to be fabricated using standard CMOS foundry processes, enabling seamless integration with existing semiconductor manufacturing infrastructure. Each pixel is engineered to independently modulate key process parameters through embedded microscale actuators and electrodes. Temperature control is achieved via lithographically patterned resistive micro-heaters, with either unipolar or PIN-configured doped silicon structures

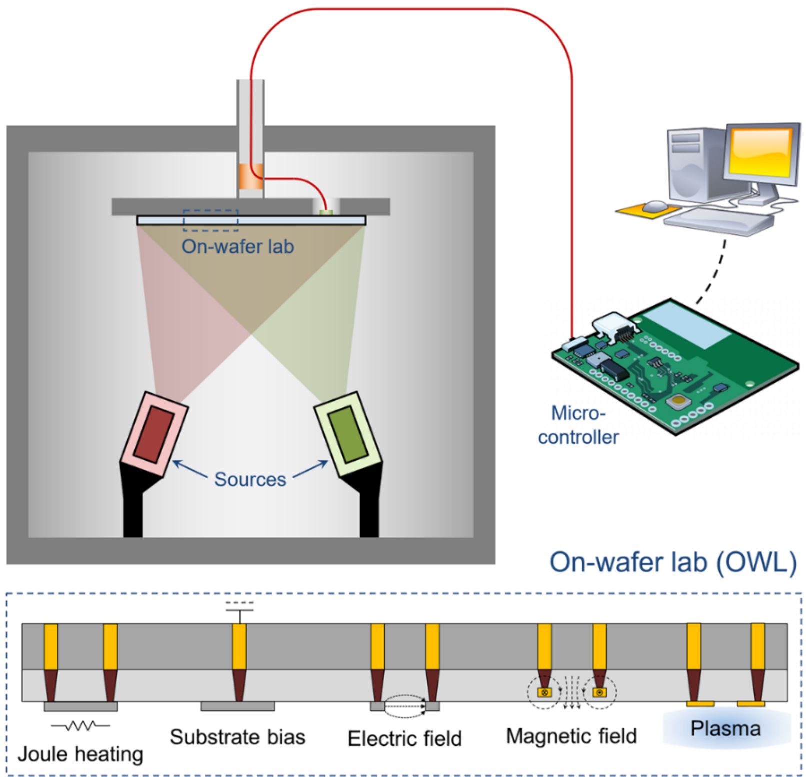

Fig. 1. An embodiment of the OWL platform enabling high-throughput combinatorial exploration for thin film deposition process development

serving as efficient, CMOS-compatible heating elements. Substrate biasing and electric field modulation can be implemented by routing voltage signals through backend metal interconnects or doped Si electrodes. The multi-level metallization available in modern CMOS processes enables precise spatial patterning of fields and supports sophisticated control of three-dimensional electric and magnetic field distributions at the wafer surface, where magnetic fields can be introduced through patterned current loops or microcoils embedded in the backend stack [20,21]. Plasma environments can be locally generated by applying radio-frequency (RF) signals to exposed electrode structures, a technique demonstrated in microscale plasma sources for on-chip chemical processing [22,23]. Control of the pixels can be achieved through either external multichannel source meters or integrated on-wafer CMOS electronics, with potential for wireless actuation and data acquisition using inductive coupling or mm-wave communication schemes. This design flexibility allows OWL to be tailored to diverse experimental setups while maintaining compatibility with high-volume wafer-scale tools.

In addition to streamlining process development, the OWL platform directly addresses many of the integration constraints that currently limit the adoption of advanced materials in semiconductor manufacturing. Its ability to apply spatially localized processing allows high-temperature steps such as epitaxial growth, crystallization anneals or dopant activation to be confined to microscale regions, leaving the surrounding wafer at BEOL-compatible temperatures. This capability enables the backend integration of materials such as ferroelectrics and magnetic oxides, whose properties critically depend on high-temperature processing [24,25], while maintaining substrate temperatures within the global BEOL thermal budget—or even lower limits when required by more stringent integration constraints. Beyond thermal control, OWL also supports *in*

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situ electric field application during deposition or annealing (poling), an emerging technique shown to influence phase formation and domain orientation in ferroelectric thin films [24]. Furthermore, OWL's architecture facilitates combinatorial plasma exposure, enabling local variation of plasma power and bias across the wafer to systematically screen process windows and assess plasma-material interactions. This approach can help resolve plasma compatibility issues that often emerge during the integration of 2D materials or low-k dielectrics [25,26]. In addition, OWL enables new modes of selective thin film growth, where localized heating [27–30] or plasma introduction can spatially induce precursor decomposition or adsorption, effectively eliminating the need for subsequent etch patterning.

3. Concept demonstration

To validate the feasibility and versatility of the OWL framework, we have fabricated and tested prototype platforms based on die-level chips diced from full wafers processed in standard CMOS foundries. These chip-scale implementations preserve the core architectural principles of OWL (such as lithographically defined, electrically addressable microstructures integrated into standard CMOS process stacks) while offering practical advantages for early-stage development and testing. While full wafer-scale integration remains the long-term goal, chip-level platforms serve as a critical steppingstone by enabling rapid prototyping, streamlined metrology, and compatibility with prototyping tools commonly used in academic and research settings. Moreover, in many advanced applications, chip-scale implementations are not merely transitional but functionally essential. For example, modules designed for massively parallel *in situ* transmission electron microscopy (TEM) must conform to the stringent spatial constraints of the sample chamber, rendering full-wafer formats infeasible. In such cases, OWL—functioning as a modular on-chip lab—provides localized process control and high-throughput experimentation within the physical limits of specialized instrumentation.

Figure 2 presents a chip-scale module for high-throughput screening of *in situ* film growth and post-deposition annealing temperatures. The chip contains a 2D array of individually addressable doped silicon microheaters fabricated on a silicon-on-insulator (SOI) wafer platform, mounted within a custom-designed ceramic carrier. Compared to prior implementations using refractory metal or polysilicon heaters [15–19], the SOI-based design offers several distinct advantages: compatibility with standard CMOS foundry processes, improved thermal stability with reduced susceptibility to resistance drift, mechanical deformation, or failure [31,32], enhanced temperature uniformity through inverse-designed doping profiles [33], and intrinsic compatibility with Si-based electronic and photonic components without introducing contamination or optical loss [34]. Electrical interfacing is achieved via a ribbon cable and vacuum feedthrough, which connect the chip to a custom-built microcontroller located outside the processing environment, enabling multichannel bias control. All components introduced into the chamber are certified to be high-vacuum compatible, ensuring seamless integration with standard deposition systems or vacuum/inert-atmosphere chambers. Beyond providing localized heating, the microheaters also function as real-time temperature sensors by leveraging the temperature dependence of their electrical resistance, enabling closed-loop feedback control. Raman thermometry was used to calibrate heater temperatures [35], and we validated stable operation of the heaters at temperatures exceeding 900 °C. The microheater platform enables high-temperature processing steps that would otherwise exceed BEOL thermal budgets, as we have demonstrated in a recent example involving magnetooptical garnet integration [36].

While the present demonstration focuses on thermal control, the underlying hardware architecture of the OWL platform is broadly extensible to other physical modalities. The modular multi-channel control system, vacuum-compatible construction, and foundry-processed microscale "pixel" structures provide a generic and scalable foundation for integrating localized

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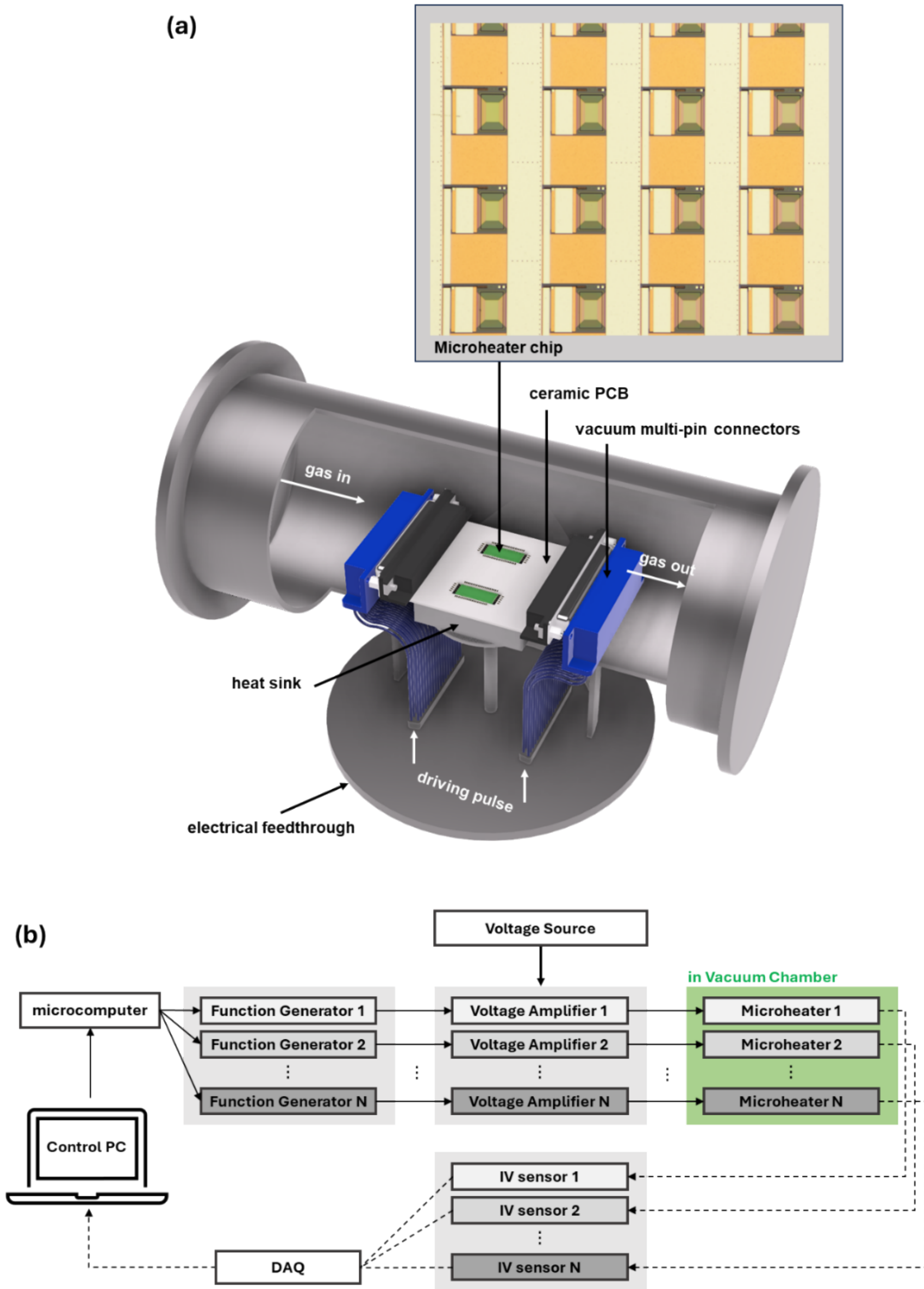

Fig. 2. Schematic and control architecture of a chip-scale OWL module for high-throughput thermal processing. (a) Design of a vacuum chamber integrating a ceramic-packaged microheater array chip with 300 μm pitch size. Insets show the packaged chip and microheater array fabricated using CMOS-compatible processes. (b) Home-built control and measurement setup enabling independent biasing, actuation, and temperature readout of each microheater.

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electric, magnetic, optical, and plasma control capabilities, thereby extending OWL's applicability well beyond thermal processing and enabling new frontiers in semiconductor processing.

4. Future outlook

The EMPOWEr framework introduces a new class of tools for accelerating semiconductor process development and enabling the integration of emerging materials. Ongoing advances in AI-guided process optimization, automated control architectures, and physics-informed inverse modeling are expected to further enhance the EMPOWEr platform, enabling more precise pixel engineering, closed-loop experimentation, and data-rich workflows that support broader adoption across both academic research and industrial manufacturing.

For photonic platforms, EMPOWEr addresses persistent integration challenges associated with temperature-sensitive material systems, where thermal processing governs crystallinity, defect density, grain structure, and phase formation, and thereby sets device-level performance. In epitaxial or quasi-epitaxial systems such as III–V semiconductors integrated on silicon for on-chip lasers and ferroelectric $BaTiO_3$ thin films for high-speed electro-optic modulators, growth and annealing temperatures critically influence crystalline quality, interface defects, and strain relaxation, directly impacting optical gain, propagation loss, and modulation bandwidth. In contrast, many functional oxides relevant to photonics, including transparent conducting oxides used as active electrodes or epsilon-near-zero (ENZ) media [37,38] and magneto-optical garnets such as Bi-substituted iron garnets for nonreciprocal components form polycrystalline films [34,36], where phase purity, grain size, and texture depend sensitively on thermal history and often evolve within narrow processing windows. EMPOWEr enables rapid, parallel exploration of these thermally defined process spaces, allowing optimal recipes to be identified efficiently across diverse photonic materials, with localized high-temperature access providing the additional benefit of compatibility with existing backend integration constraints. An exciting future direction for the EMPOWEr framework lies in its integration with AI-driven and automated experimentation workflows [39,40]. One of the most persistent bottlenecks in applying machine learning to semiconductor process development is the scarcity of high-quality, high-dimensional experimental datasets [41]. While advanced algorithms offer significant promise for guiding process optimization, their performance is fundamentally constrained by the volume, diversity, and fidelity of the data they are trained on. Conventional foundry fabrication workflows produce sparse datasets due to the cost and time of sequential process runs, compounded by tool availability and limited wafer throughput. In contrast, OWL enables the generation of rich datasets by systematically varying process parameters across thousands of spatially addressable micro-environments on a single chip or wafer. This inherently parallelized approach not only accelerates data acquisition but also enhances statistical robustness, facilitating the development of more predictive and generalizable AI models. EMPOWEr also allows AI models to make connections between final properties and processing conditions, which are often just as important, if not more so, than the intrinsic properties of the materials. Moreover, because each data point is obtained under tightly controlled, localized conditions using industry-standard substrates, the resulting datasets are ideally suited for use in multimodal learning frameworks and digital twin platforms. As AI models continue to evolve, OWL-based platforms may serve as foundational infrastructure for closed-loop, autonomous process development pipelines.

Another promising direction for future development lies in the application of advanced inverse design algorithms to optimize the physical architectures of OWL pixels across multiple domains. The ability to independently control temperature, electric and magnetic fields, plasma exposure, and optical excitation within microscale environments presents a complex, high-dimensional design challenge, one that traditional parameter sweeps or heuristic tuning struggle to address efficiently. Inverse design offers a powerful alternative by enabling designers to define desired

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spatial distributions or performance targets and then computationally discover viable pixel geometries that meet those specifications. This approach not only accelerates the design cycle but also reveals the fundamental limits of achievable configurations under given fabrication constraints. Recent work has demonstrated inverse-designed microheaters with tailored thermal profiles [33], and similar strategies can be extended to engineer localized electric field gradients, magnetic actuation profiles, and even microplasma confinement. Such co-design approaches are particularly attractive for materials with intrinsic polarization or magnetization, such as ferroelectric $BaTiO_3$ or magneto-optical materials, where coupled control of thermal, electric, or magnetic fields can directly influence domain structure and functional response. As these algorithms grow more sophisticated and physics-aware, they are expected to play a central role in maximizing the precision, flexibility, and functional density of future OWL implementations.

Beyond accelerating conventional process development, the spatially controlled microenvironments enabled by the OWL framework offer a unique opportunity to unlock entirely new classes of material processing techniques, many of which have traditionally required complex, dedicated instrumentation. For instance, OWL's ability to generate localized spatial or temporal thermal gradients can enable seeded (pseudo-)single-crystal growth, as demonstrated in GeSn alloys and oxide glasses under carefully tuned heat treatment [42,43]. The platform also lends itself naturally to techniques such as zone melting and directional solidification, where localized heating elements can be dynamically actuated to guide solid-liquid interfaces with sub-millimeter precision. The capacity to independently modulate local thermal or plasma activation conditions further opens the door to selective area deposition of multilayer films with varied layer sequences across a single substrate without complex masking. Such a capability, for example, enables simultaneous fabrication of two-dimensional material heterostructures such as MoS_2/WS_2, $MoSe_2/WSe_2$, and graphene/transition metal dichalcogenides, which underpin waveguide-integrated photodetectors, electro-absorption modulators, and nonlinear optical elements [44–46]. Moreover, the extremely low thermal mass and short thermal decay times of microheaters make OWL ideally suited for implementing rapid thermal annealing or quenching protocols, potentially enabling metastable phase formation or defect engineering with nanosecond-level thermal control. The application of intense local electric or magnetic fields, which can be orders of magnitude higher than those attainable with conventional macroscopic equipment, also enables new modalities in field-directed growth, particularly for ferroelectric and magnetic materials where domain structure and orientation are field-sensitive. Together, these capabilities point to a future in which OWL not only expedites established fabrication workflows, but also enables fundamentally new processing science, previously inaccessible due to the limitations of traditional instrumentation.

Moving forward, the same principles that underpin EMPOWEr point to a broader paradigm shift: harnessing advanced semiconductor microsystem technologies to empower the development of semiconductor technologies themselves. This self-reinforcing approach positions EMPOWEr as a foundational platform for next-generation semiconductor technology innovations.

Funding. National Science Foundation (2328839).

Acknowledgement. Funding support is provided by the National Science Foundation under Award 2328839. J. F. Lim is thankful for the support from the CN Yang Scholars Programme at Nanyang Technological University.

Disclosures. The authors declare no conflicts of interest.

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